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COHEN, PONTANI, LIEBERMAN & PAVANE LLP
551 FIFTH AVENUE
SUITE 1210
NEW YORK, NY 10176

EXAMINER	
CAMPBELL, SHAUN M	

ART UNIT	PAPER NUMBER
2829	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/566,955	HARLE, VOLKER	
	Examiner	Art Unit	
	SHAUN CAMPBELL	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2010* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

FINAL ACTION

1. Amendment, received 3/1/2010, has been entered into the record.

2. Claims 1-5 and 7-15 are presented for examination. Claim 1 is currently amended and claims 2-5 and 7-15 are previously presented.

Drawings

3. The drawings were received on 3/1/2010. These drawings are accepted.

Claim Objections

4. Claim 15 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 15 does not further limit claim 4 because claim 4 is dependent on claim 1 which includes the same limitation in claim 15.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-5 and 7-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haerle (US Patent No. 6,100.104) in view of Tokunaga et al. (US Patent No. 5,659,184) hereafter referred to as Tokunaga.

7. As to claims 1 and 15, Haerle discloses a method for the production of a plurality of optoelectronic semiconductor chips (a plurality of light emitting diode chips 100 as shown in figs 5-6) each having a structural element with each structural element comprising a semiconductor layer sequence (fig 5, layers 21, 22, and 23; col. 7, lines 1-5; structural element is the layers 21-23), the method comprising the steps of:

providing a chip composite base (fig 1-3 substrate wafer 19) comprising a substrate (fig 1-5, growth substrate wafer 3) and a growth surface (fig 1, the main surface 9);

forming on the growth surface a mask material layer (fig 1, mask layer 4) with a multiplicity of windows (fig 3, mask openings 10), wherein a mask material is chosen in so that a semiconductor material of the semiconductor layer that is to be grown in a later method step essentially cannot grow on said mask material or can grow in a substantially worse manner in comparison with the growth surface (col. 6, lines 55-67);

essentially simultaneously growing semiconductor layers to form the structural elements on regions of the growth surface that lie within the windows (fig 4);

singulating the chip composite base applied material to form semiconductor chips each having a plurality of the structural elements (col. 7, lines 33-36; figs 5-6, the structural element is the layers 21-23); and

wherein, after the growth of the semiconductor layers (fig 5 is performed after fig 4), a layer made of electrically conductive contact material that is transmissive (front-side contact metallization layer 15, fig 5; it is transimissive because it would either bounce the radiation when a non-transparent material is used or pass the radiation through when a transparent material is used) to an electromagnetic radiation emitted by the active zone (fig 4, light-emitting active layer 23) is applied to the semiconductor layers.

However, Haerle fails to disclose wherein the optoelectronic semiconductor chips each have a plurality of structural elements with each structural element comprising a semiconductor layer sequence; and

most of the windows have an average extent less than or equal to 1 micrometer.

Nonetheless, Tokunaga discloses wherein the optoelectronic semiconductor chips each have a plurality of structural elements with each structural element comprising a semiconductor layer sequence (col. 4, lines 45-67);

the semiconductor layers of a plurality of structural elements are electrically conductively connected to one another by a contact material (fig 15G, one dimensional LED array with electrode 1507); and

most of the windows have an average extent less than or equal to 2 micrometers (col. 12, lines 25-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the method of making long lasting LEDs and laser diodes as is taught by Haerle to make an LED array head or a large-sized monolithic display

device or a one-dimensional LED array as is taught by Tokunaga since it is shown that instead of always cutting the LEDs into individual LED chips, as is taught by Haerle, it is possible to use an array of LEDs in a display device such as in a numerical display device (Tokunaga, col. 1, lines 44-49).

And, In Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device.

8. As to claims 2-5, 7, 8 and 12-14, Haerle in view of Tokunaga discloses the method as claimed in claim 1 (paragraph above).

Haerle further discloses wherein the chip composite base (fig 1-3, substrate wafer 19) has at least one semiconductor layer grown epitaxially onto the substrate (col. 6, line 55 to col. 7, line 5) and the growth surface is a surface on that side of the epitaxially grown semiconductor layer (fig 4, the bottom side of 21 is in contact with the main surface 9) which is remote from the substrate (col. 6, lines 52-53)[claim 2].

wherein the chip composite base (fig 1-3, substrate wafer 19) has a semiconductor layer sequence grown epitaxially onto the substrate (col. 6, line 55 to col. 7, line 5) with an active zone that emits electromagnetic radiation (fig 4, light-emitting active layer 23), and the growth surface is a surface on that side of the semiconductor

layer sequence (fig 4, the bottom side of 21 is in contact with the main surface 9) which is remote from the substrate (col. 6, lines 52-53)[claim 3].

wherein the structural elements respectfully have an epitaxially grown semiconductor layer sequence (col. 6, line 55 to col. 7, line 5) with an active zone that emits electromagnetic radiation (fig 4, light-emitting active layer 23)[claim 4].

wherein the mask material has SiO2 or Al2O3 (col. 6, lines 38-39)[claim 5].

wherein the average thickness of the mask material layer (fig 9, mask layer 4) is less than the cumulated thickness of the semiconductor layers of a structural element (fig 9, semiconductor layer sequence 18)[claim 7].

wherein the mask material layer is at least partly removed after the growth of the semiconductor layers (col. 7, lines 13-20)[claim 8].

wherein the growth conditions for the growth of the semiconductor layers are at least one of set and varied during growth in such a way that semiconductor layers of the structural elements form a lens-shaped form, a truncated cone-shaped form, or a polyhedral form (col. 7, lines 66-67)[claim 12].

wherein the semiconductor layers are grown by means of metal organic vapor phase epitaxy (col. 6, lines 55-67)[claim 13].

an optoelectronic semiconductor chip, characterized in that it is produced according to a method as claimed in claim 1 (col. 7, lines 33-36)[claim 14]

9. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haerle in view of Tokunaga, and further in view of Braun (US Patent No. 6,110,277).

10. As to claims 9-11, Haerle in view of Sugiyama discloses the method as claimed in claim 1 (paragraphs above).

Haerle in view of Tokunaga does not explicitly disclose

wherein, after the growth of the semiconductor layers, a planarization layer is applied over the growth surface [claim 9];

wherein a material whose refractive index is lower than that of the semiconductor layers is chosen for the planarization layer [claim 10]; or

wherein a dielectric material is chosen for the planarization layer [claim 11].

Nonetheless, these features are well known in the art and would have been an obvious modification of the method disclosed by Haerle in view of Tokunaga, as evidenced by Braun.

Braun discloses wherein, after the growth of the semiconductor layers, a planarization layer is applied over the growth surface (fig 5, passivation layer 60)[claim 9] to protect the light-emitting diode;

wherein a material whose refractive index is lower than that of the semiconductor layers is chosen for the planarization layer (fig 5, the passivation layer 60 must have a refractive index that is lower than the semiconductor layers to allow the radiation to pass through, otherwise the radiation is blocked and the light-emitting diode could not shine)[claim 10]; and

wherein a dielectric material is chosen for the planarization layer (any material has dielectric properties, including the passivation layer 60)[claim 11].

Given the teaching of Braun, a person having ordinary skills in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Haerle in view of Tokunaga by employing the well known or conventional features of a lower refractive index planarization layer, such as disclosed by Braun, in order to make a light-emitting diode with good efficiency and optimized green, blue, and violet spectral region.

Response to Arguments

11. Applicant's arguments filed 3/1/2010 have been fully considered but they are not persuasive.

12. Applicant's argued in substance that Haerle cannot have a contact metallization layer 15 that electrically conductively connects multiple semiconductor layer of non-existent plural structural elements in its optoelectronic chip.

13. Examiner traverses this argument because Haerle does disclose a contact metallization layer 15 that electrically conductively connects to the LEDs and Tokunaga has been previously combined with Haerle to teach that the LEDs are arranged into an array with the multiple LEDs connected together by an electrode in order to use the LEDs in a display device such as in a numerical display device.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SHAUN CAMPBELL whose telephone number is (571)270-3830. The examiner can normally be reached on Monday Through Thursday 7:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nguyen Ha can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Shaun Campbell/
Examiner, Art Unit 2829
4/21/10

/Ha T. Nguyen/
Supervisory Patent Examiner, Art Unit 2829